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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,602	RANKIN ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17-19, 22, 24-26, 32, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong (U.S. 6,340,556).

Regarding claim 17, Wong teaches a method, comprising:

- providing a semiconductor structure, wherein the semiconductor structure comprises a photoresist layer on a semiconductor substrate (column 6, lines 23-25);
- forming a plurality of features in the photoresist layer (column 8, lines 7-10);
- measuring a plurality of critical dimensions of the plurality of features to determine at least one critical dimension error for at least one feature of the plurality of features (column 9, lines 33-38);
- determining from said at least one critical dimension error a dose of electron beam exposure to correct the at least one critical dimension error for the at least one feature of the plurality of features (column 8, lines 14-67); and
- correcting the at least one critical dimension error by selectively exposing only the at least one feature comprising the critical dimension error to an

electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature (Wong teaches exposing the remaining photoresist layer, which is made up of only the features requiring correction, to an electron beam in order to reduce the linewidth of the features—column 8, lines 7-67).

Regarding claim 24, Wong teaches a method, comprising:

- providing a mask photoresist layer (column 6, lines 23-25; column 1, lines 30-31 teach using the photoresist as an etch mask);
- forming a plurality of features in the mask photoresist layer (column 8, lines 7-10);
- measuring a plurality of critical dimensions of the plurality of features in the mask photoresist layer to determine at least one critical dimension error for at least one feature of the plurality of features (column 9, lines 33-38);
- determining from said at least one critical dimension error a dose of electron beam exposure to correct the at least one critical dimension error for the at least one feature of the plurality of features (column 8, lines 14-67); and
- correcting the at least one critical dimension error by selectively exposing only the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one

feature (Wong teaches exposing the remaining photoresist layer, which is made up of only the features requiring correction, to an electron beam in order to reduce the linewidth of the features—column 8, lines 7-67).

Regarding claims 18 and 25, Wong teaches the method of claims 17 and 24, and further teaches that the dose of electron beam exposure comprises a power level of the electron beam for a specified amount of time (column 8, lines 36-39—Wong teaches a preferred beam energy, which is power multiplied by an amount of time).

Regarding claims 19 and 26, Wong teaches the method of claims 17 and 24, and further teaches that correcting the critical dimension error comprises decreasing a size of the at least one feature (column 8, lines 55-57).

Regarding claim 22, Wong teaches the method of claim 17. Wong further teaches forming an electrical component in a space in the semiconductor device that is defined by the at least one feature (column 3, lines 40-41).

Regarding claims 32 and 33, Wong teaches the method of claims 17 and 24, and further teaches that said determined dose of electron beam exposure comprises multiple emissions of an electron beam for a specified amount of time (column 9, lines 32-33 teach using a uniform dose distribution, indicating multiple electron beam emissions for some amount of time).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 8, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838).

Regarding claim 1, Wong teaches a method, comprising:

- providing a first semiconductor device;
- analyzing the first semiconductor device to determine at least one critical dimension error within the first semiconductor device (column 9, lines 33-38);
- determining from said at least one critical dimension error a dose of electron-beam exposure to correct the at least one critical dimension error in a process (column 8, lines 14-67), comprising:
- providing a semiconductor structure, wherein the semiconductor structure comprises a photoresist layer on a semiconductor substrate (column 6, lines 23-25);
- forming a plurality of features in the photoresist layer (column 8, lines 7-10), wherein at least one feature of the plurality of features comprises the at least one critical dimension error; and
- correcting the at least one critical dimension error by selectively exposing only the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure (Wong teaches exposing the remaining photoresist layer, which

is made up of only the features requiring correction, to an electron beam in order to reduce the linewidth of the features—column 8, lines 7-67).

Wong does not teach that the process to correct the at least one critical dimension error is a process to correct the at least one critical dimension area on a second semiconductor device during a subsequent process.

Marella teaches a method of analyzing a first semiconductor device to determine at least one critical dimension error (paragraph 0033 teaches that one of the defects encompassed by the invention is a lateral structure that has a dimension either smaller or larger than predetermined values; paragraph 0045) and use the analysis to alter a parameter on a process instrument to repair defects and reduce the number of defects in subsequent devices (paragraph 0016, last two sentences).

Therefore, at the time of the invention, it would have been obvious to modify the method taught by Wong by applying the dose of electron-beam exposure to correct the at least one critical dimension error during a subsequent process on a second device, as taught by Marella, rather than on the original device, as taught by Wong. The motivation for doing so at the time of the invention would be to avoid propagating systematic errors such as a defect in the photomask, as taught by Marella (paragraph 0006).

Regarding claim 2, Wong and Marella together teach the method of claim 1. Wong further teaches that the dose of electron beam exposure comprises a power level of the electron beam for a specified amount of time (column 8, lines 36-39—Wong teaches a preferred beam energy, which is power multiplied by an amount of time).

Regarding claim 3, Wong and Marella together teach the method of claim 1. Wong further teaches that correcting the critical dimension error comprises decreasing a size of the at least one feature (column 8, lines 55-57).

Regarding claim 5, Wong and Marella together teach the method of claim 1. Wong further teaches that analyzing comprises measuring a plurality of critical dimensions within the first semiconductor device to determine the at least one critical dimension error (column 9, lines 33-38).

Regarding claim 8, Wong and Marella together teach the method of claim 1. Wong further teaches forming an electrical component in a space in the second semiconductor device that is defined by the at least one feature (column 3, lines 40-41).

Regarding claim 28, Wong and Marella together teach the method of claim 1. Wong further teaches that said determined dose of electron beam exposure comprises multiple emissions of an electron beam for a specified amount of time (column 9, lines 32-33 teach using a uniform dose distribution, indicating multiple electron beam emissions for some amount of time).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) as applied to claim 1 above, and further in view of Cowan (U.S. 6,605,951).

Regarding claim 6, Wong and Marella together teach the method of claim 1, but do not teach that analyzing comprises performing a functionality test of the first semiconductor device to determine a plurality of operating conditions for a plurality of electrical components within the first semiconductor device.

Cowan teaches that it is common to analyze semiconductor devices wherein said analyzing comprises performing a functionality test of the semiconductor device to determine a plurality of operating conditions for a plurality of electrical components within the first semiconductor device (column 1, line 15 – column 3, line 14).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong and Marella together, and further use the device-analysis method taught by Cowan to determine operating conditions for electrical components within the semiconductor device, since Cowan teaches that it is conventional to do so.

Claims 10-12, 15, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1, 2000).

Regarding claim 10, Wong teaches a method, comprising:

- providing a semiconductor structure, wherein the semiconductor structure comprises a photoresist layer on a semiconductor substrate (column 6, lines 23-25);
- propagating radiation to expose the photoresist layer to form a plurality of features in the photoresist layer (column 7, lines 5-7), and then measuring on the substrate a plurality of critical dimensions within the pattern to determine at least one critical dimension error within said pattern (column 9, lines 33-38);

- determining from said at least one critical dimension error a dose of electron-beam exposure that will be used to correct the at least one critical dimension error for the at least one feature comprising the at least one critical dimension error (column 8, lines 14-67); and
- correcting the critical dimension error by selectively exposing only the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron-beam exposure that corrects the critical dimension error of the at least one feature (Wong teaches exposing the remaining photoresist layer, which is made up of only the features requiring correction, to an electron beam in order to reduce the linewidth of the features–column 8, lines 14-67).

Wong does not teach using a mask to pattern the photoresist layer or measuring on the mask the plurality of critical dimension errors.

Wolf et al. teaches that it common to expose photoresist through a mask to pattern the photoresist (p. 489, first paragraph).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong and further pattern the photoresist layer by exposing it through a mask, as taught by Wolf to be a common method of patterning photoresist.

Wolf et al. additionally teaches measuring critical dimension errors on a mask (section 13.8.5 on pp. 626-627). Wolf et al. teaches that such a step is an effective

means of predicting critical dimension errors on a device, since defects or mistakes in the mask pattern will be imparted to the device (last paragraph on p. 626).

Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to use the method taught by Wong and further analyze the mask for critical dimension errors, as taught by Wolf et al., instead the substrate, since Wolf teaches that this is an effective means of predicting critical dimension errors on a device.

Regarding claim 11, Wong and Wolf et al. together teach the method of claim 10. Wong further teaches that the dose of electron beam exposure comprises a power level of the electron beam for a specified amount of time (column 8, lines 36-39—Wong teaches a preferred beam energy, which is power multiplied by an amount of time).

Regarding claim 12, Wong and Wolf et al. together teach the method of claim 10. Wong further teaches that correcting the critical dimension error comprises decreasing a size of the at least one feature (column 8, lines 55-57).

Regarding claim 15, Wong and Wolf et al. together teach the method of claim 10. Wong further teaches forming an electrical component in a space in the semiconductor device that is defined by the at least one feature (column 3, lines 40-41).

Regarding claim 31, Wong and Wolf et al. together teach the method of claim 10. Wong further teaches that said determined dose of electron beam exposure comprises multiple emissions of an electron beam for a specified amount of time (column 9, lines 32-33 teach using a uniform dose distribution, indicating multiple electron beam emissions for some amount of time).

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838), as applied to claim 1 above, and further in view of Ghandhi (*VLSI Fabrication Principles—Silicon and Gallium Arsenide*, Second Edition, 1994).

Regarding claim 7, Wong and Marella together teach the method of claim 1. Wong additionally teaches that the at least one feature includes a first feature and a second feature (column 8, lines 11-13 teaches photoresist lines), but does not teach forming a trench in a space in the semiconductor substrate that is located between the first and second features.

Ghandhi teaches that forming a trench between features in a semiconductor device is a way to achieve electrical isolation (section 11.3.1, pp. 719-721). Since Wong teaches that the photoresist lines form microelectronic device images (column 3, lines 40-41), it would have been obvious to one of ordinary skill in the art at the time of the invention to additionally form a trench between the photoresist lines in order to electrically isolate the microelectronic devices from each other, as taught by Ghandhi.

Regarding claim 9, Wong and Marella together teach the method of claim 8 (note 35 U.S.C. 103(a) rejection above). They do not expressly teach that the electrical component is selected from the group consisting of a transistor, a resistor, a wire, a diode, and a capacitor.

Ghandhi teaches the use of photolithography and photoresist features to form a wire (metal pattern—see Fig. 10.8 and pp. 683-684).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong and Marella together, and further form a wire from the photoresist feature, since Ghandhi teaches that this is a common use of photoresist features.

Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1, 2000) as applied to claims 10 and 15 above, and further in view of Ghandhi (*VLSI Fabrication Principles—Silicon and Gallium Arsenide*, Second Edition, 1994).

Regarding claim 14, Wong and Wolf et al. together teach the method of claim 10 (note 35 U.S.C. 103(a) rejection above). Wong additionally teaches that the at least one feature includes a first feature and a second feature (column 8, lines 11-13 teaches photoresist lines), but does not teach forming a trench in a space in the semiconductor substrate that is located between the first and second features.

Ghandhi teaches that forming a trench between features in a semiconductor device is a way to achieve electrical isolation (section 11.3.1, pp. 719-721). Since Wong teaches that the photoresist lines form microelectronic device images (column 3, lines 40-41), it would have been obvious to one of ordinary skill in the art at the time of the invention to additionally form a trench between the photoresist lines in order to electrically isolate the microelectronic devices from each other, as taught by Ghandhi.

Regarding claim 16, Wong and Wolf together teach the method of claim 15 (note 35 U.S.C. 103(a) rejection above). They do not expressly teach that the electrical

component is selected from the group consisting of a transistor, a resistor, a wire, a diode, and a capacitor.

Ghandhi teaches the use of photolithography and photoresist features to form a wire (metal pattern—see Fig. 10.8 and pp. 683-684).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong and Marella together, and further form a wire from the photoresist feature, since Ghandhi teaches that this is a common use of photoresist features.

Claims 21 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Ghandhi (*VLSI Fabrication Principles—Silicon and Gallium Arsenide*, Second Edition, 1994).

Regarding claim 21, Wong teaches the method of claim 17 (note 35 U.S.C. 102(b) rejection above). Wong additionally teaches that the at least one feature includes a first feature and a second feature (column 8, lines 11-13 teaches photoresist lines), but does not teach forming a trench in a space in the semiconductor substrate that is located between the first and second features.

Ghandhi teaches that forming a trench between features in a semiconductor device is a way to achieve electrical isolation (section 11.3.1, pp. 719-721). Since Wong teaches that the photoresist lines form microelectronic device images (column 3, lines 40-41), it would have been obvious to one of ordinary skill in the art at the time of the invention to additionally form a trench between the photoresist lines in order to electrically isolate the microelectronic devices from each other, as taught by Ghandhi.

Regarding claim 23, Wong teaches the method of claim 22 (note 35 U.S.C. 102(b) rejection above). Wong does not expressly teach that the electrical component is selected from the group consisting of a transistor, a resistor, a wire, a diode, and a capacitor.

Ghandhi teaches the use of photolithography and photoresist features to form a wire (metal pattern—see Fig. 10.8 and pp. 683-684).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong, and further form a wire from the photoresist feature, since Ghandhi teaches that this is a common use of photoresist features.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838), as applied to claim 1 above, and further in view of Okoroanyanwy et al. (U.S. 2002/0160628).

Regarding claim 4, Wong and Marella together teach the method of claim 1. Wong further teaches that determining the dose of electron beam exposure comprises providing a relationship between a changing of critical dimension size changes and dosage of electron beam exposure; and choosing the dose of the electron beam exposure for a desired change in critical dimension size, said choosing being based on said relationship (column 8, lines 11-67; column 9, lines 32-40). Wong does not, however, expressly teach providing a graphical relationship.

Okoroanyanwy et al. teaches that it is known in the art of semiconductor device processing to provide graphical representations between a changing of critical

dimension size changes and dosage of electron beam exposure (Figs. 6-7). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong and Marella together, and further provide a graphical relationship between a changing of critical dimension size changes and dosage of electron beam exposure, since Okoroanyanwy et al. teaches that providing such a graphical relationship is known in the art of semiconductor processing as an effective method of presenting experimental data.

Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1, 2000), as applied to claim 10 above, and further in view of Okoroanyanwy et al. (U.S. 2002/0160628).

Regarding claim 13, Wong and Wolf et al. together teach the method of claim 10. Wong further teaches that determining the dose of electron beam exposure comprises providing a relation ship between a changing of critical dimension size changes and dosage of electron beam exposure; and choosing the dose of the electron beam exposure for a desired change in critical dimension size, said choosing being based on said relationship (column 8, lines 11-67; column 9, lines 32-40). Wong does not, however, expressly teach providing a graphical relationship.

Okoroanyanwy et al. teaches that it is known in the art of semiconductor device processing to provide graphical representations between a changing of critical dimension size changes and dosage of electron beam exposure (Figs. 6-7). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art

to use the method taught by Wong and Wolf together, and further provide a graphical relationship between a changing of critical dimension size changes and dosage of electron beam exposure, since Okoroanyanwy et al. teaches that providing such a graphical relationship is known in the art of semiconductor processing as an effective method of presenting experimental data.

Claims 20 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Okoroanyanwy et al. (U.S. 2002/0160628).

Regarding claims 20 and 27, Wong teaches the method of claims 17 and 24, and further teaches that determining the dose of electron beam exposure comprises providing a relationship between a changing of critical dimension size changes and dosage of electron beam exposure; and choosing the dose of the electron beam exposure for a desired change in critical dimension size, said choosing being based on said relationship (column 8, lines 11-67; column 9, lines 32-40). Wong does not, however, expressly teach providing a graphical relationship.

Okoroanyanwy et al. teaches that it is known in the art of semiconductor device processing to provide graphical representations between a changing of critical dimension size changes and dosage of electron beam exposure (Figs. 6-7). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong, and further provide a graphical relationship between a changing of critical dimension size changes and dosage of electron beam exposure, since Okoroanyanwy et al. teaches that providing such a graphical relationship is known

in the art of semiconductor processing as an effective method of presenting experimental data.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) and Cowan (U.S. 6,605,951), as applied to claim 6 above, and further in view of Lowell et al. (U.S. 5,963,783).

Regarding claim 29, Wong, Marella, and Cowan together teach the method of claim 6, but do not expressly teach that analyzing comprises comparing said plurality of operating conditions to a plurality of calculated operating conditions of the first semiconductor device.

However, Lowell et al. teaches comparing experimental semiconductor processing parameters to calculated parameters as part of an analysis procedure. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong, Marella, and Cowan together, and further compare said plurality of operating conditions to a plurality of calculated operating conditions of the first semiconductor device, since Lowell et al. teaches that it is known in the art of semiconductor device processing to compare device performance to calculations.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) and Cowan (U.S. 6,605,951), as applied to claim 6 above, and further in view of Bode et al. (U.S. 6,937,914).

Regarding claim 30, Wong, Marella, and Cowan together teach the method of claim 6, but do not teach that analyzing further comprises comparing said plurality of

operating conditions to a plurality of actual operating characteristics of a second semiconductor device known to comprise no CD errors.

Bode et al. teaches analyzing devices for critical dimension errors by comparing operating conditions of a device against the operating characteristics of other devices, some known to comprise no CD errors (Fig. 2 shows a plot of operating characteristics as a function of CD error—0 is no error; column 5, lines 35-49).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Wong, Marella, and Cowan together, and further compare a plurality of operating conditions to a plurality of actual operating characteristics of a second semiconductor device known to comprise no CD errors, as taught by Bode et al., since the method taught by Bode et al. overcomes or reduces the effects of some of the problems associated with other methods, such as lost profits due to a manufacturer's inability to fill orders in the event of diminished productivity (column 2, lines 35-54).

Response to Arguments

Applicant's arguments filed 6/26/2006 have been fully considered but they are not persuasive.

Applicant primarily argues that Wong does not anticipate the claims as amended, specifically because Wong teaches exposing more than only the feature comprising the critical dimension error. However, this argument is not persuasive because although Wong exposes all of the features of a device, they all contain critical dimension errors,

so Wong does teach selectively exposing only the features comprising a critical dimension error.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

had

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